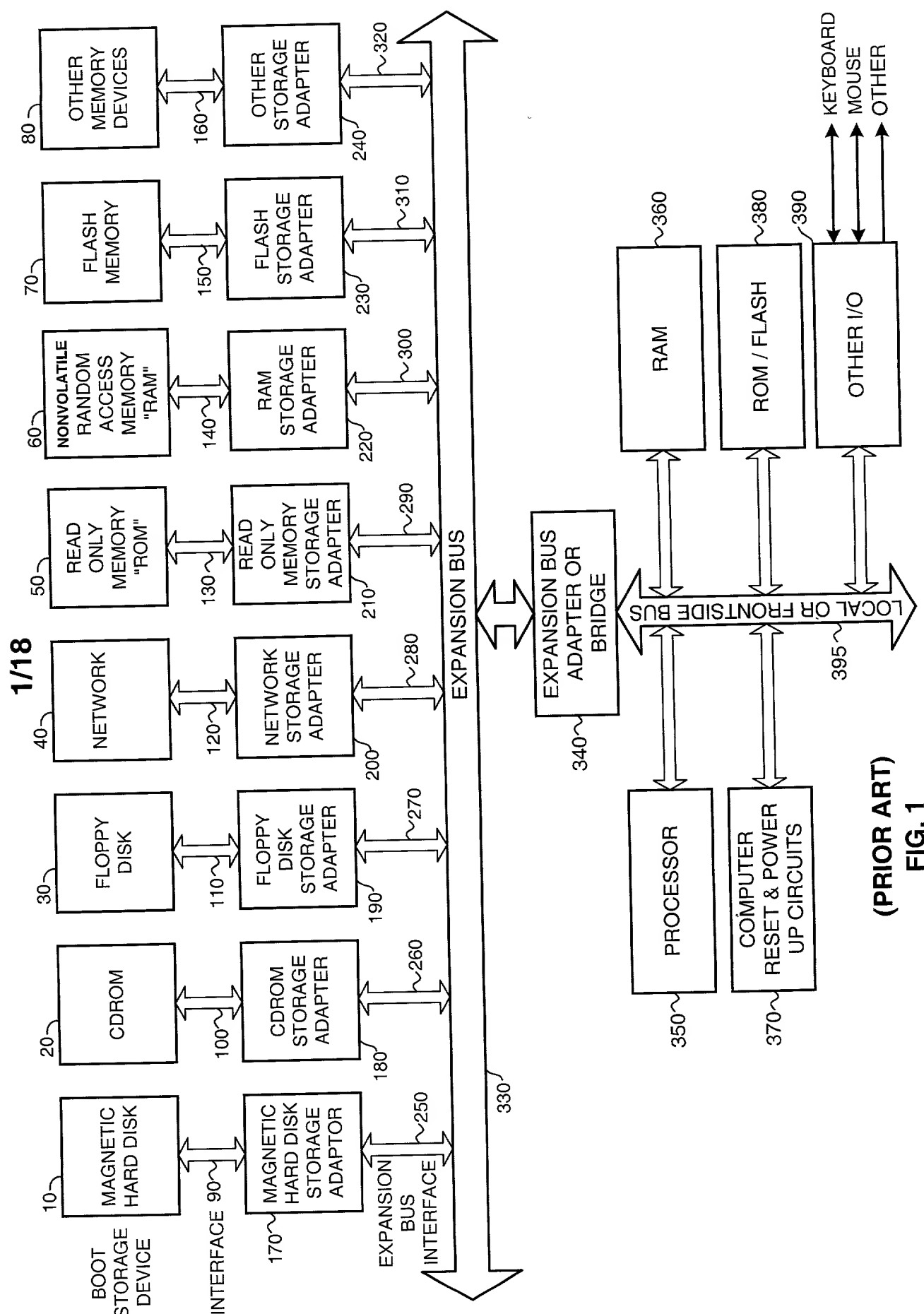
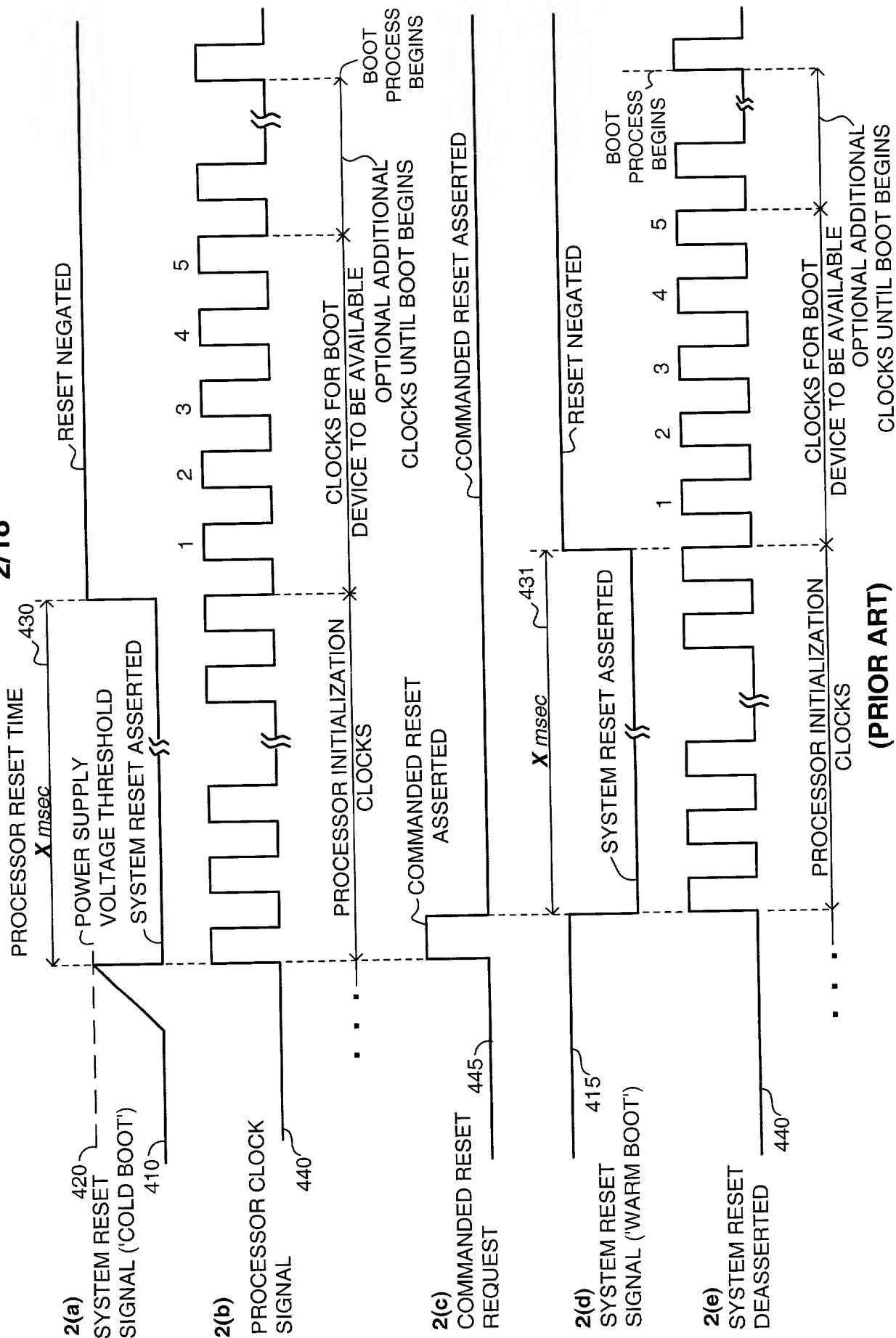


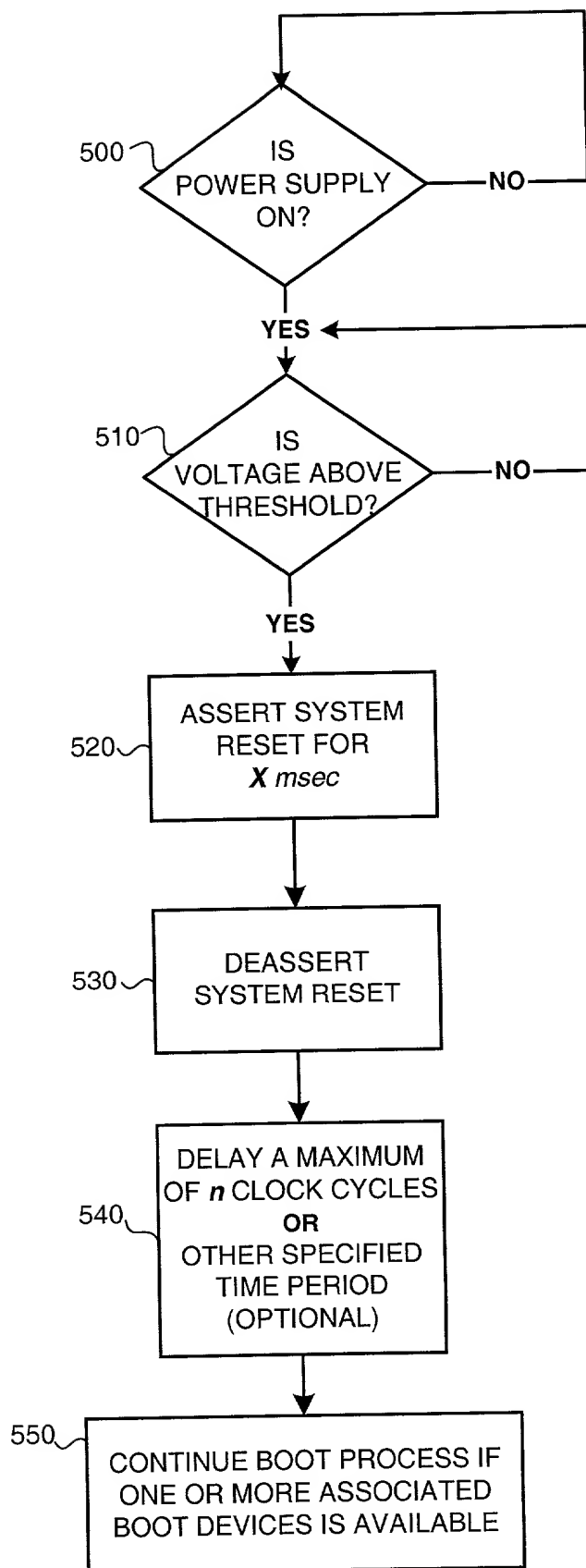
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(PRIOR ART)
FIG. 1

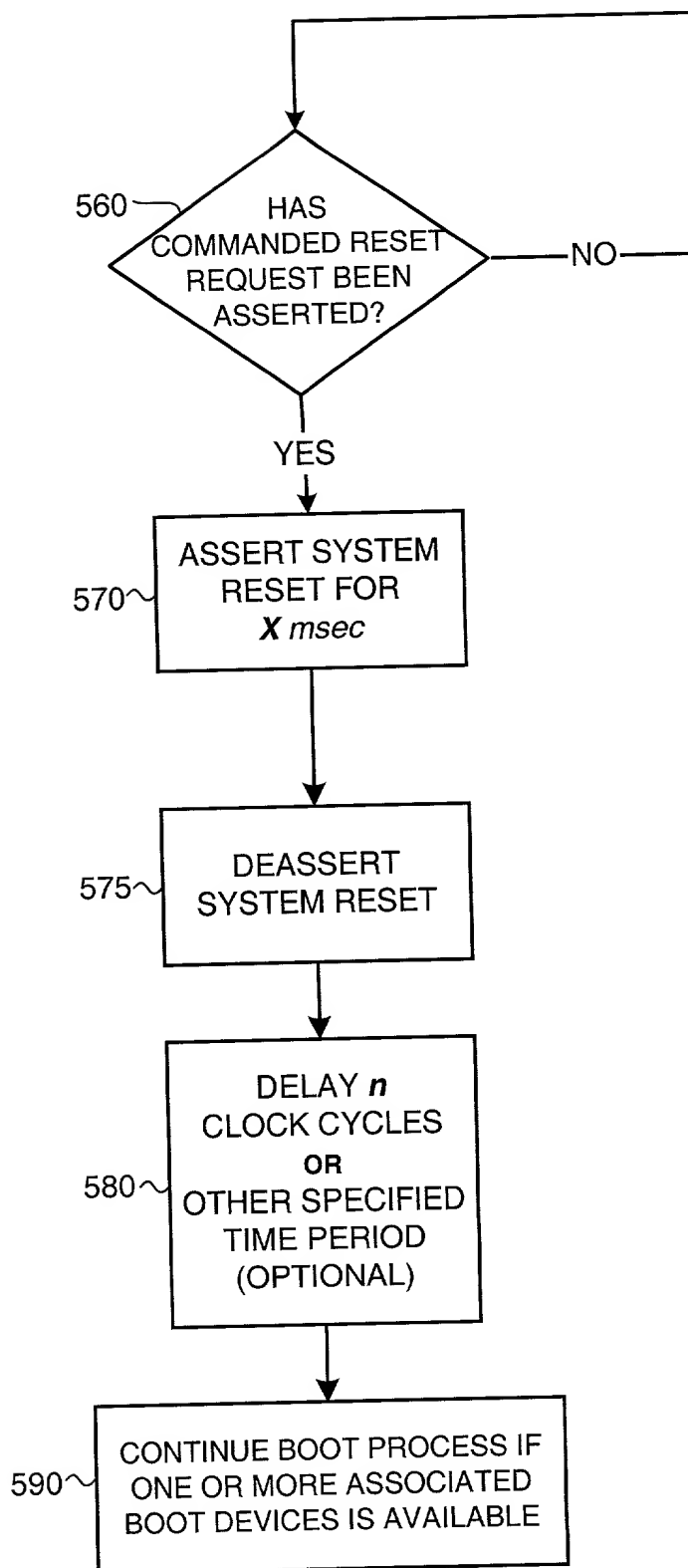


(PRIOR ART)
FIG. 2



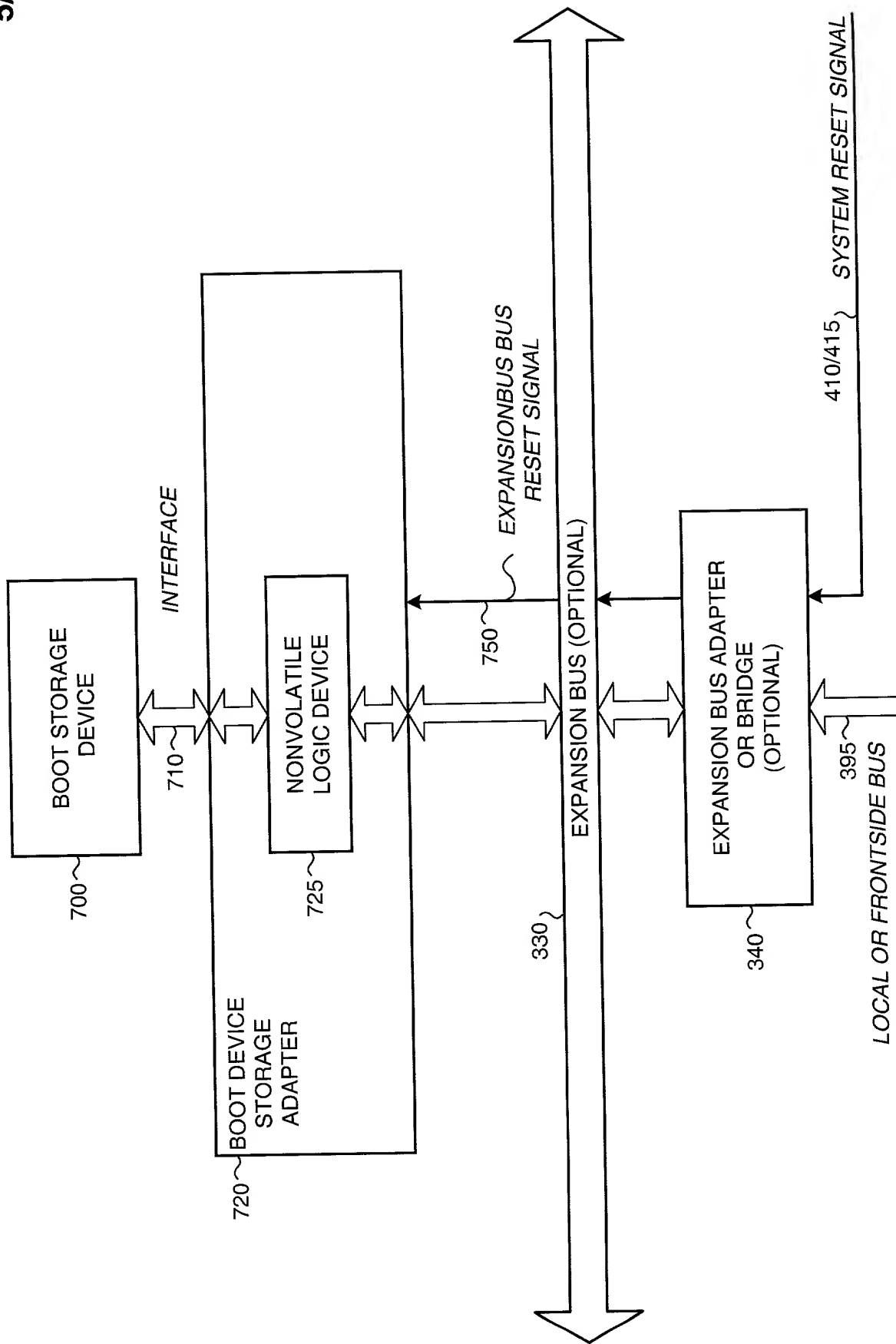
(PRIOR ART)

FIG. 3a



(PRIOR ART)

FIG. 3b



(PRIOR ART)
FIG. 4

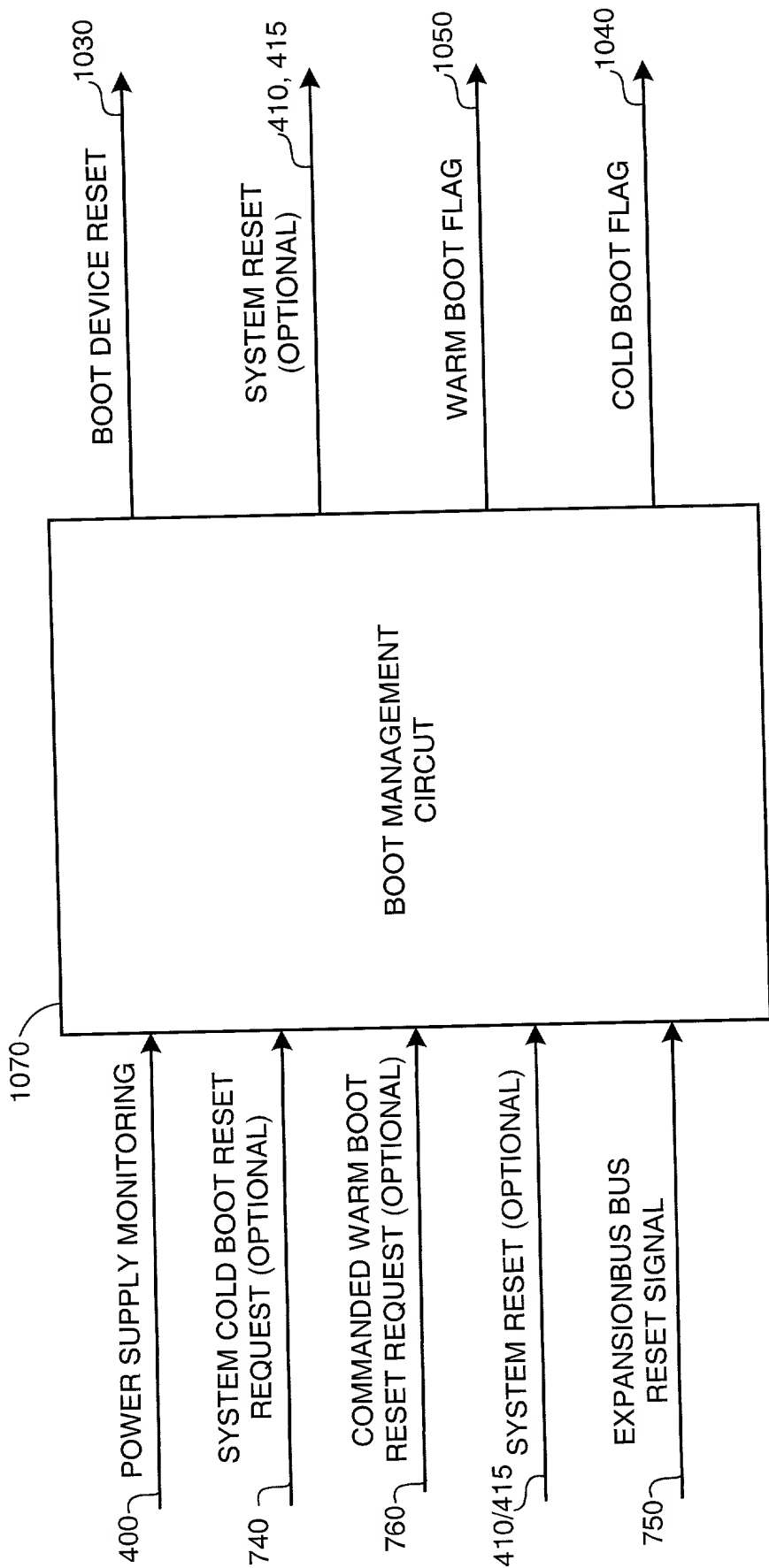


FIG. 5

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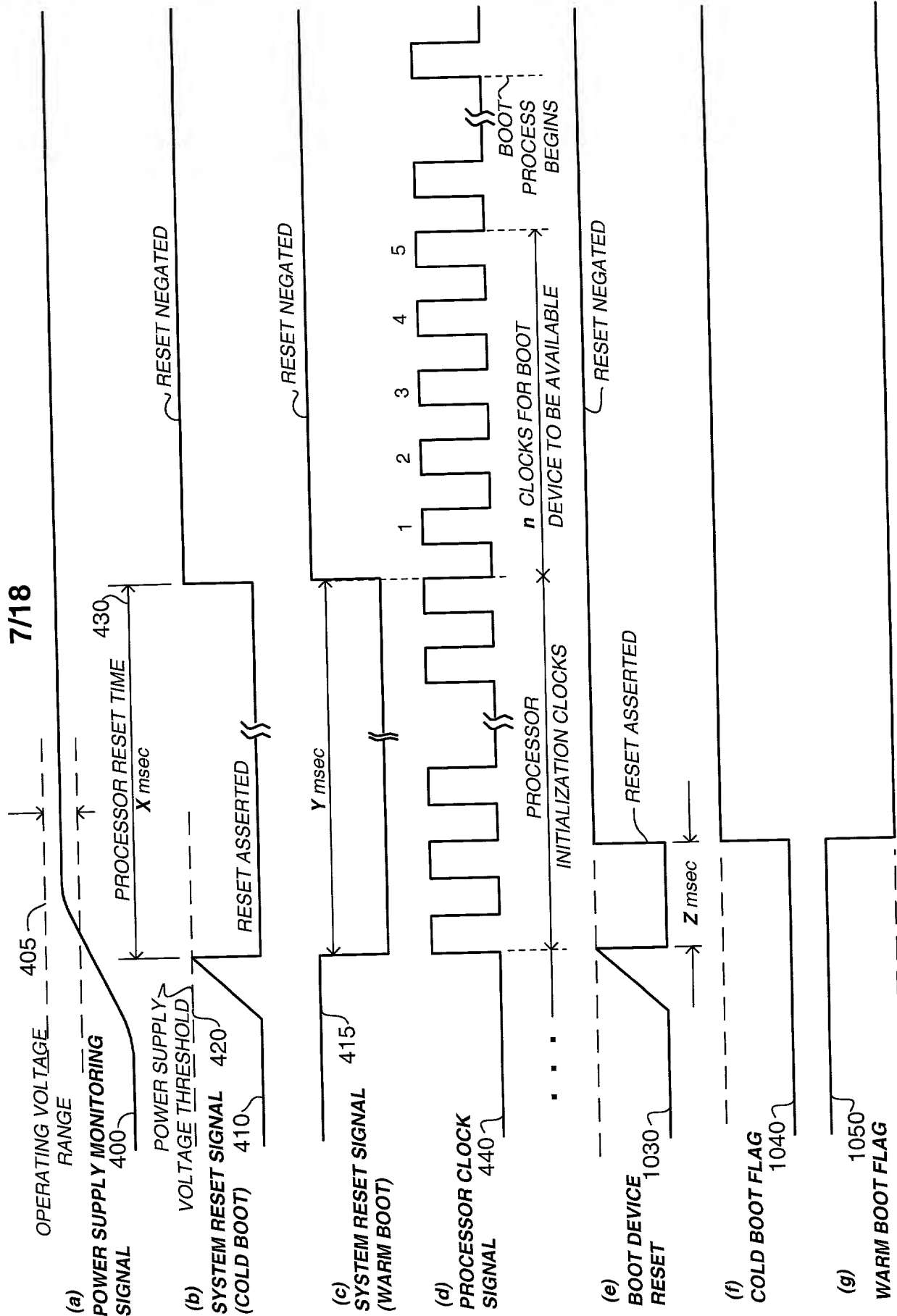


FIG. 6

FIG. 7 is a timing diagram showing the sequence of events during a system reset. The diagram includes signals for the processor clock, boot device reset, cold boot flag, warm boot flag, system cold boot reset request signal, and commanded warm boot reset request signal. The sequence starts with the processor clock (440) and the boot device reset (1030) signal. The boot device reset signal is asserted for a duration of Z msec. The cold boot flag (1040) is then set. The warm boot flag (1050) is also set. The system cold boot reset request signal (740) is then asserted. The commanded warm boot reset request signal (760) is also asserted. The sequence ends with the processor clock (440) and the boot device reset (1030) signal.

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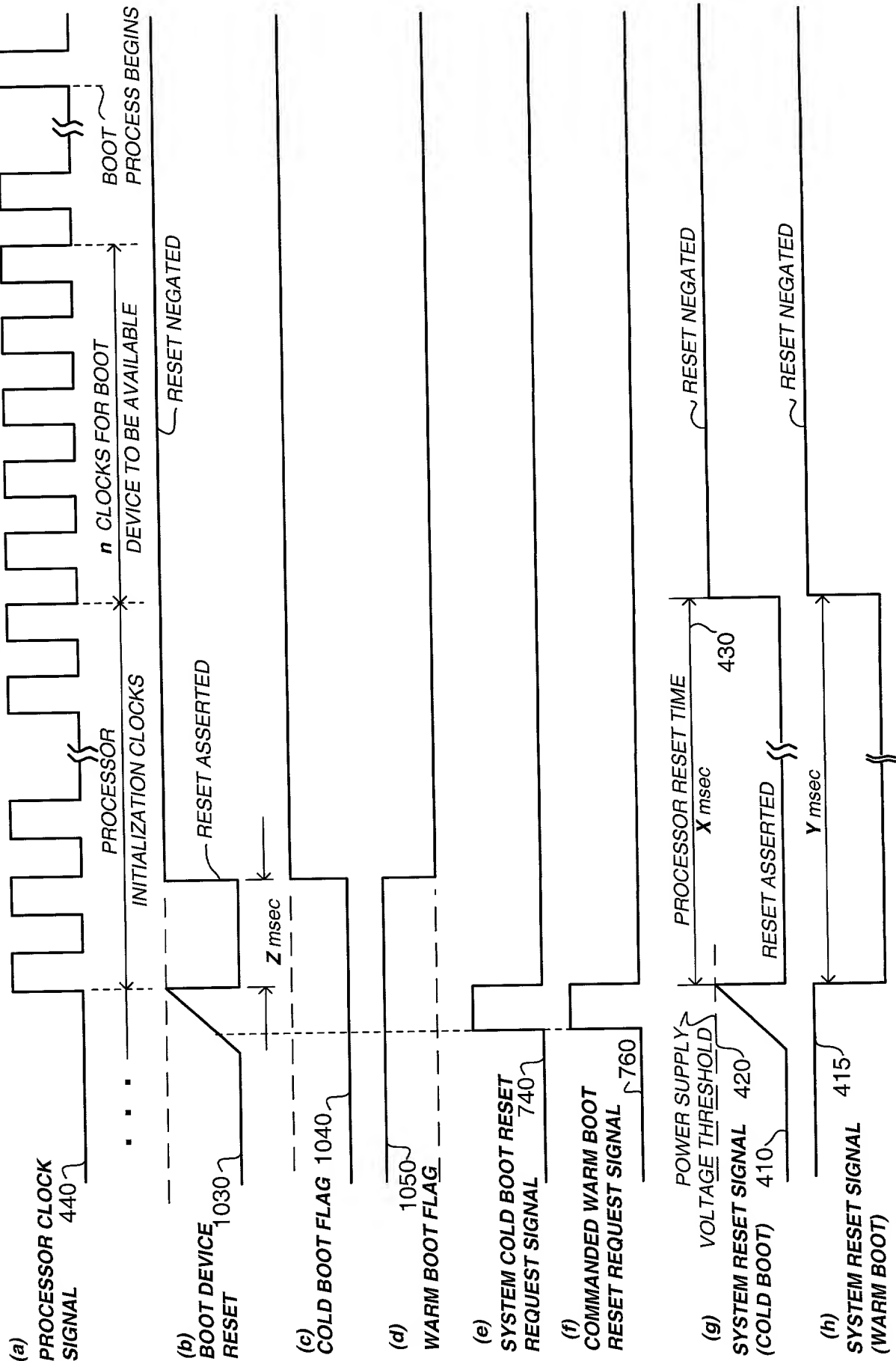


FIG. 7

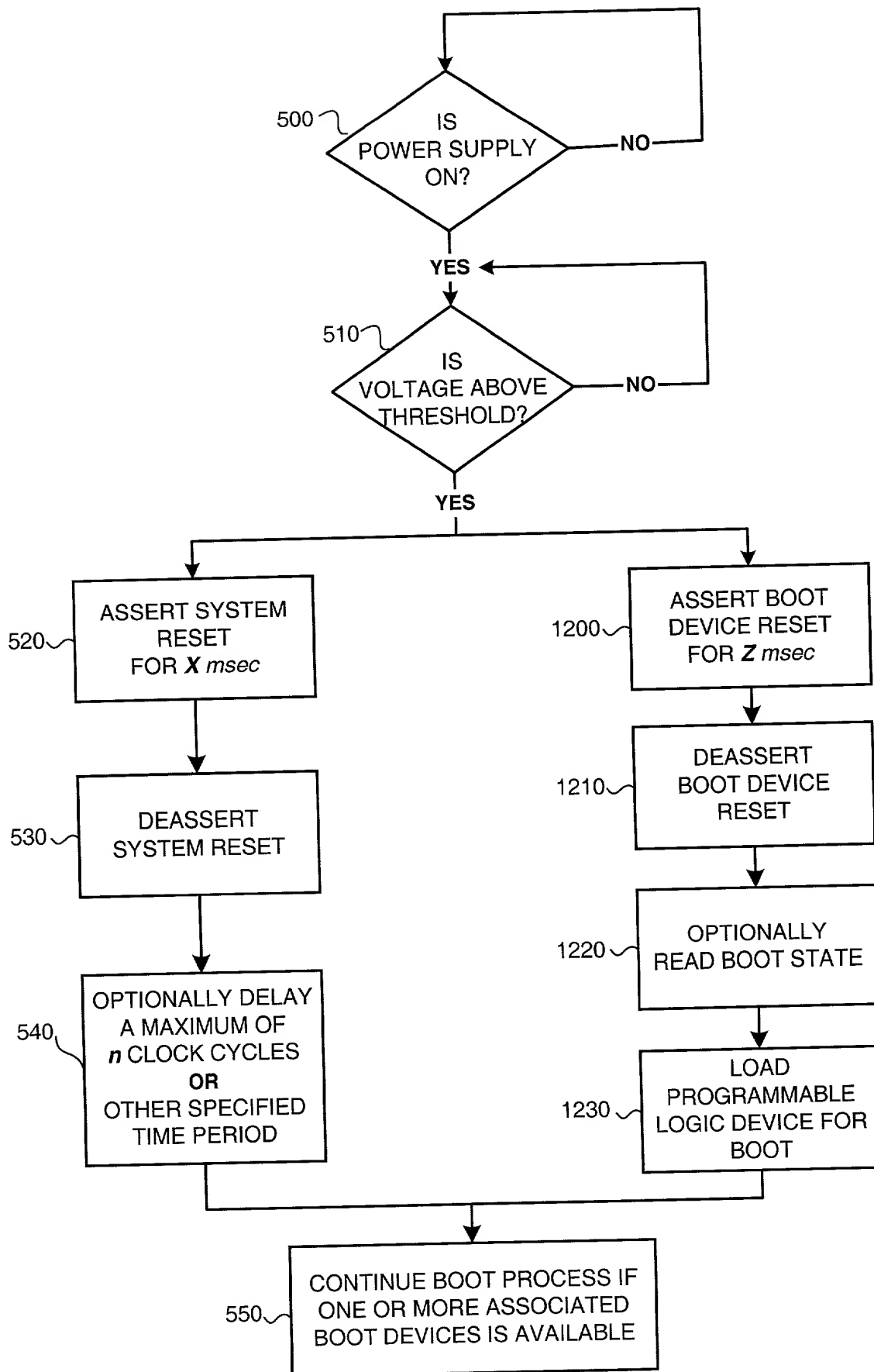


FIG. 8a

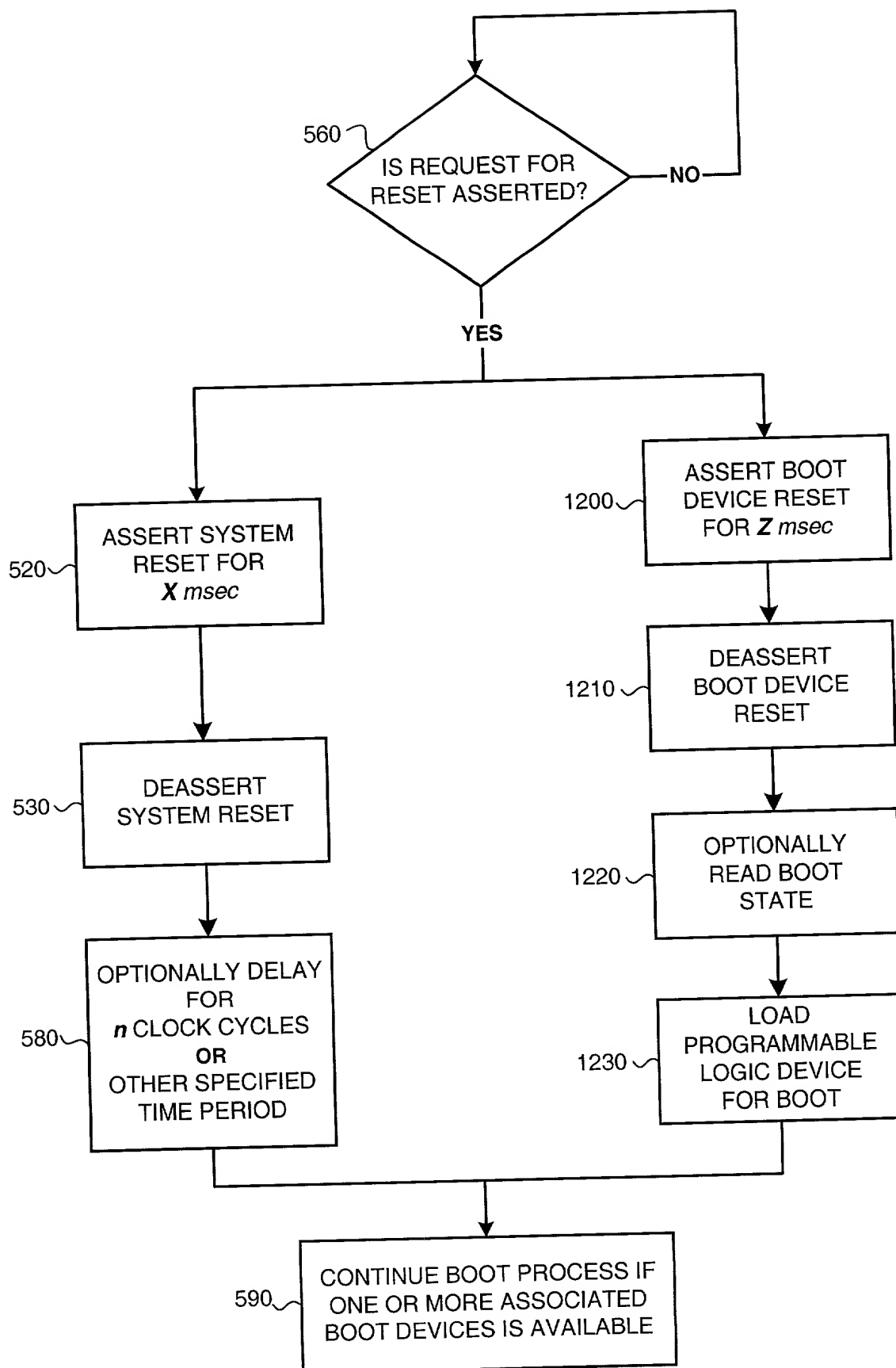


FIG. 8b

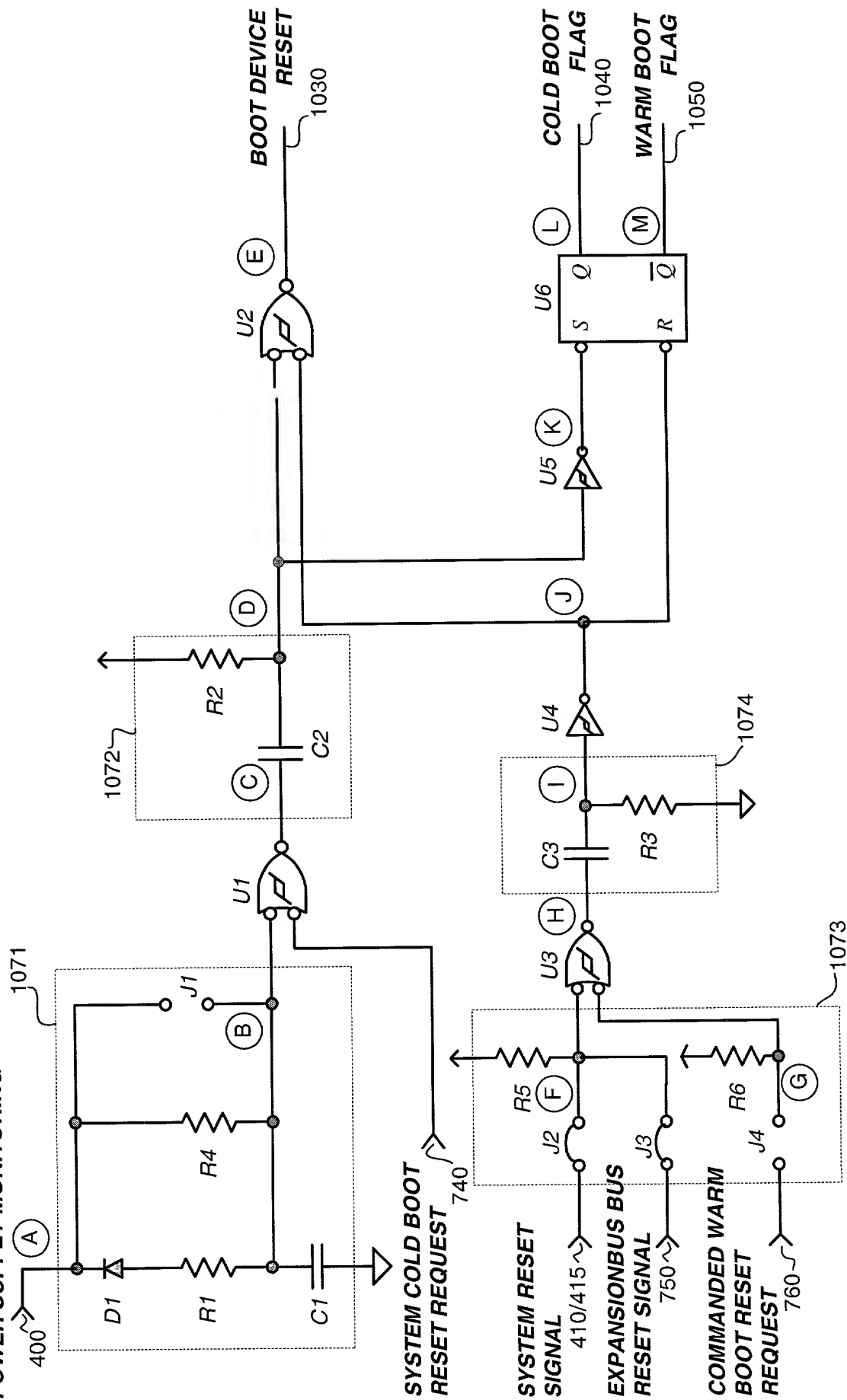


FIG. 9

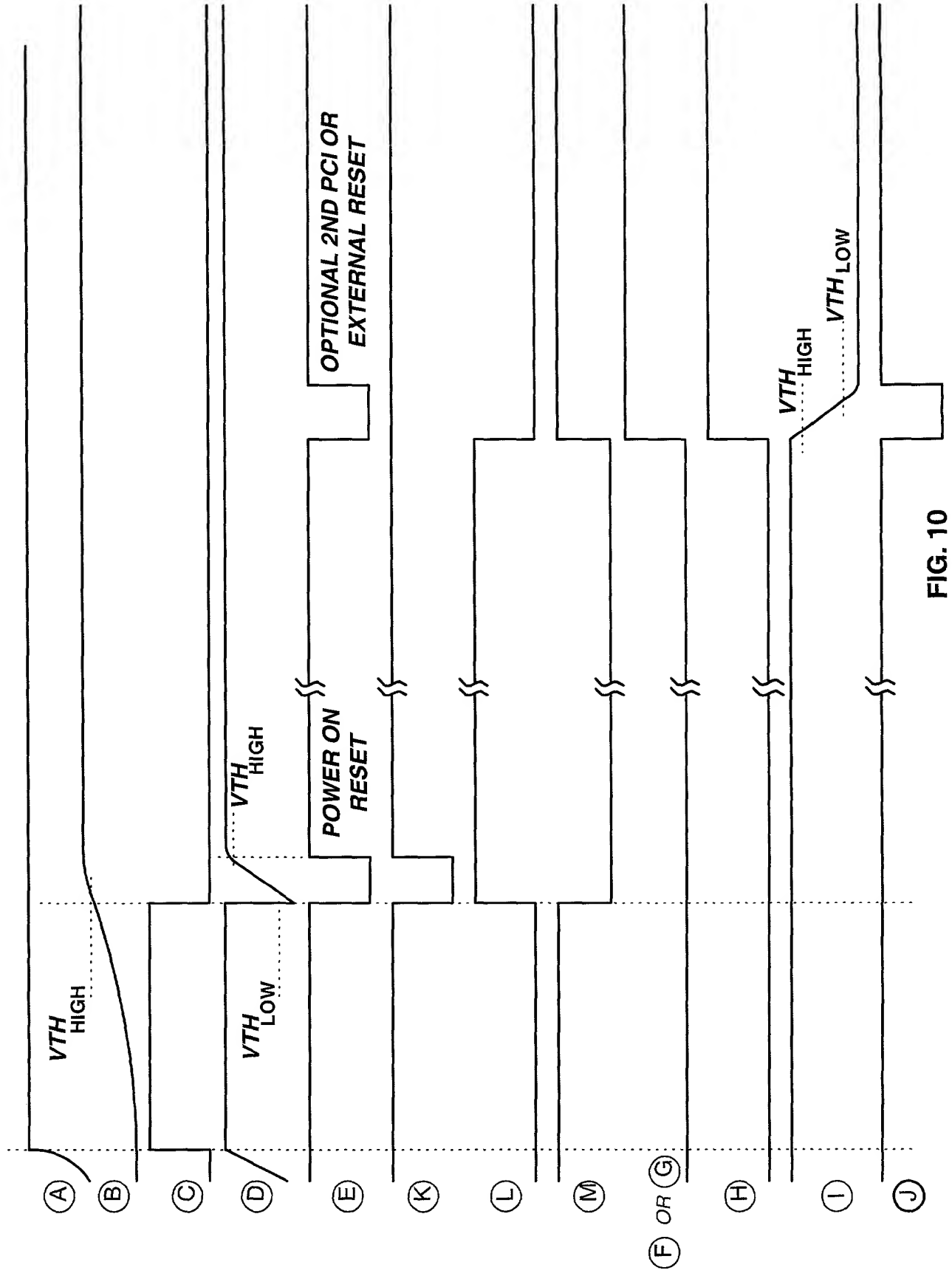


FIG. 10

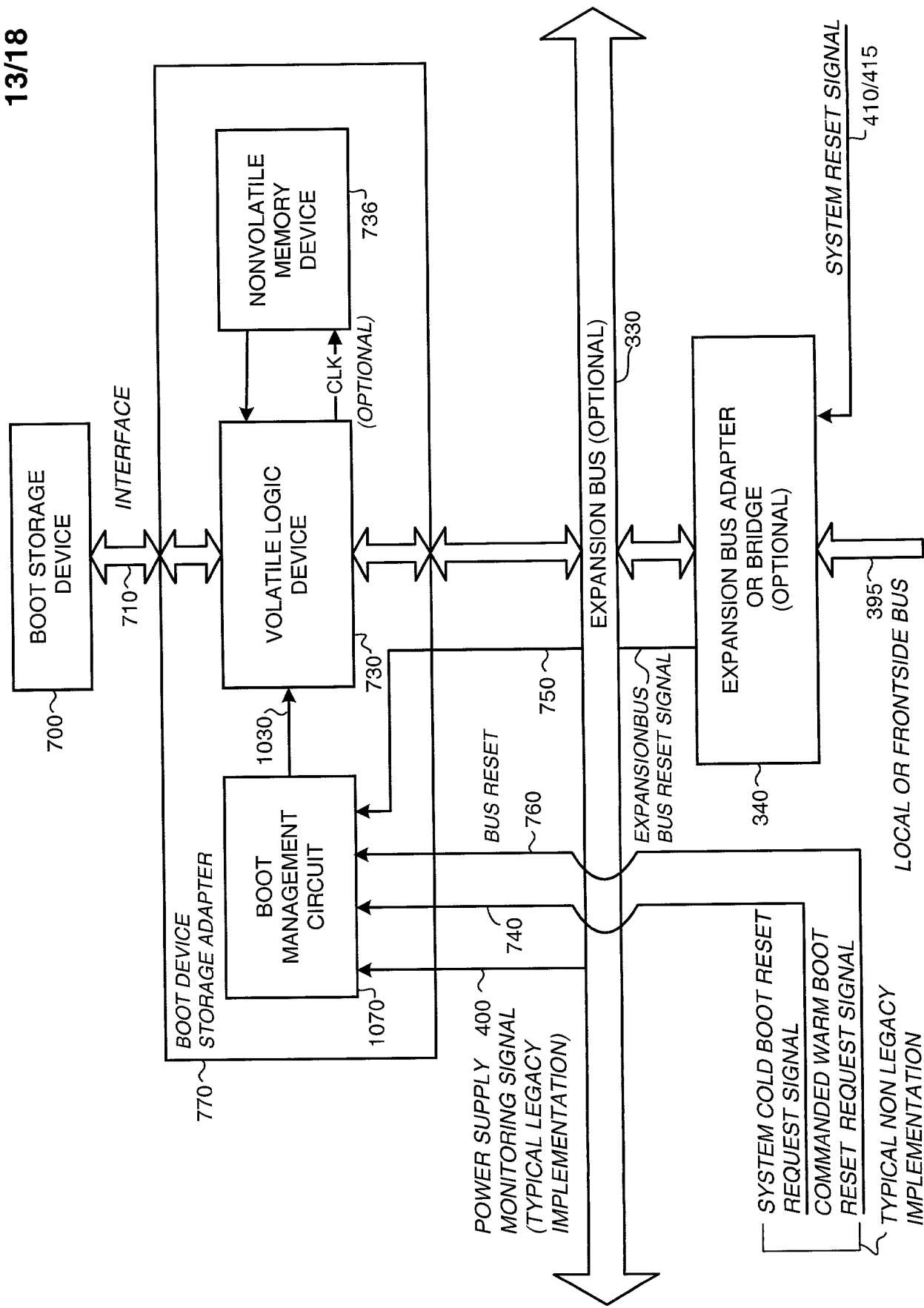


FIG. 11

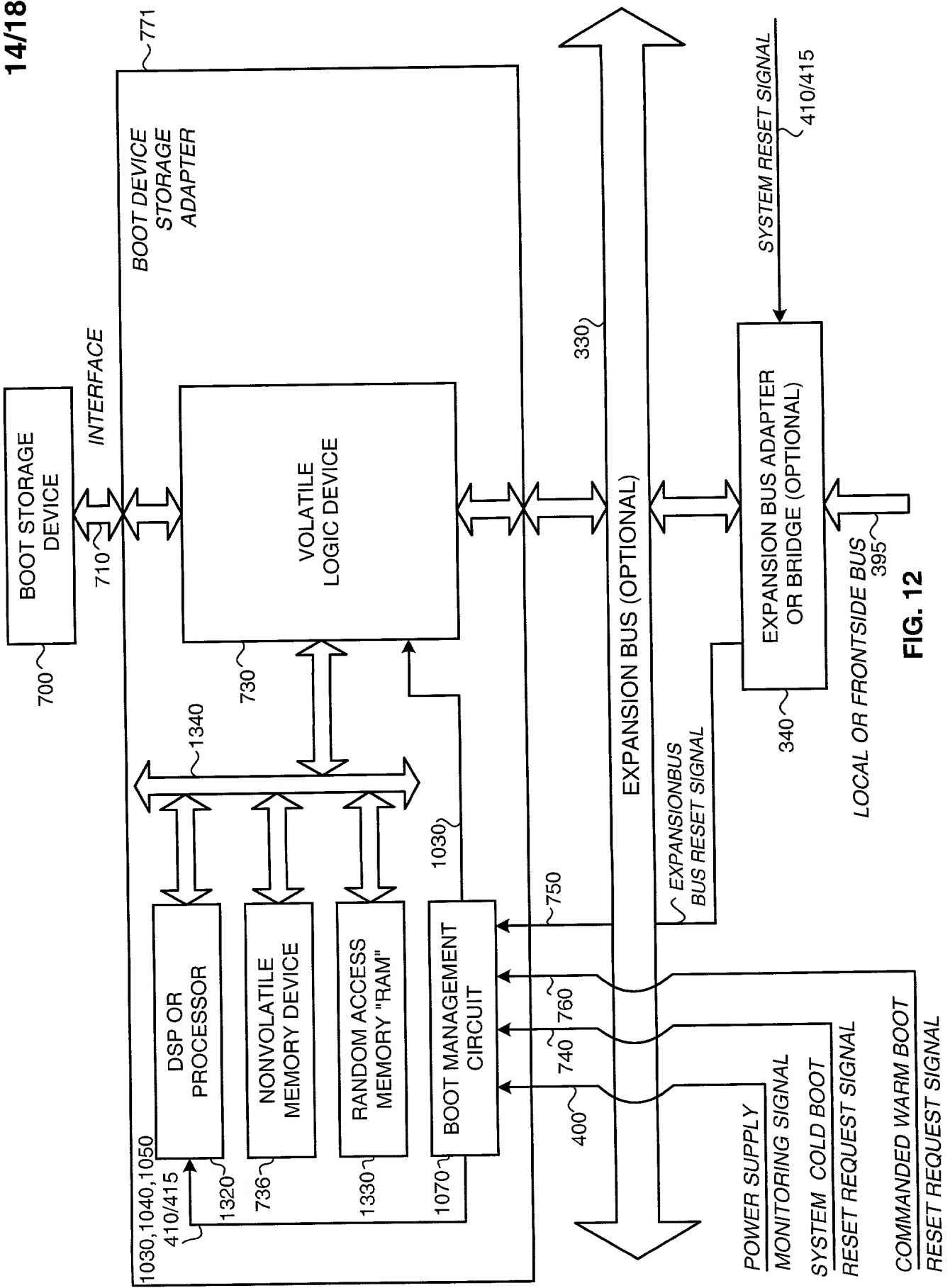


FIG. 12

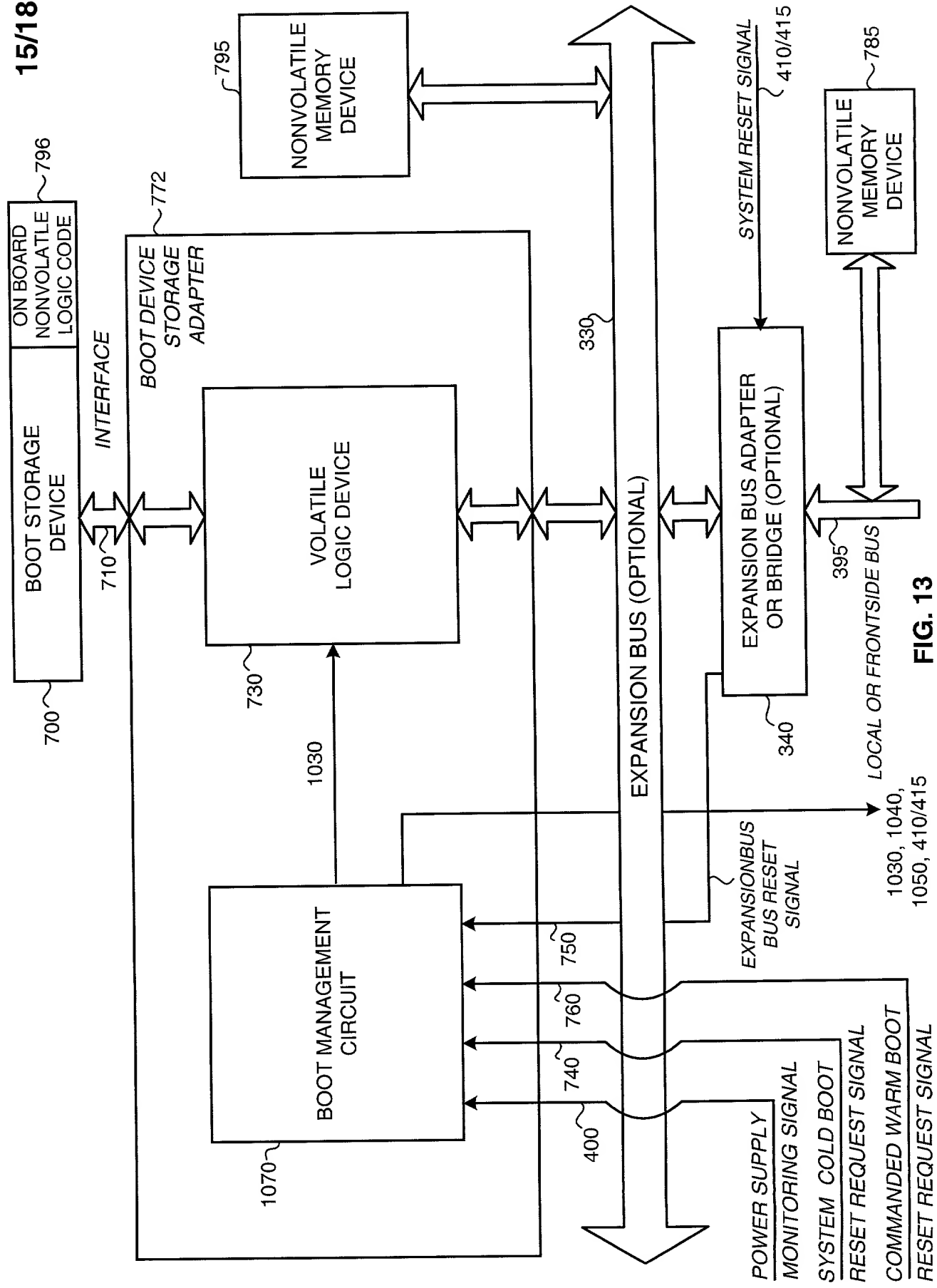


FIG. 13

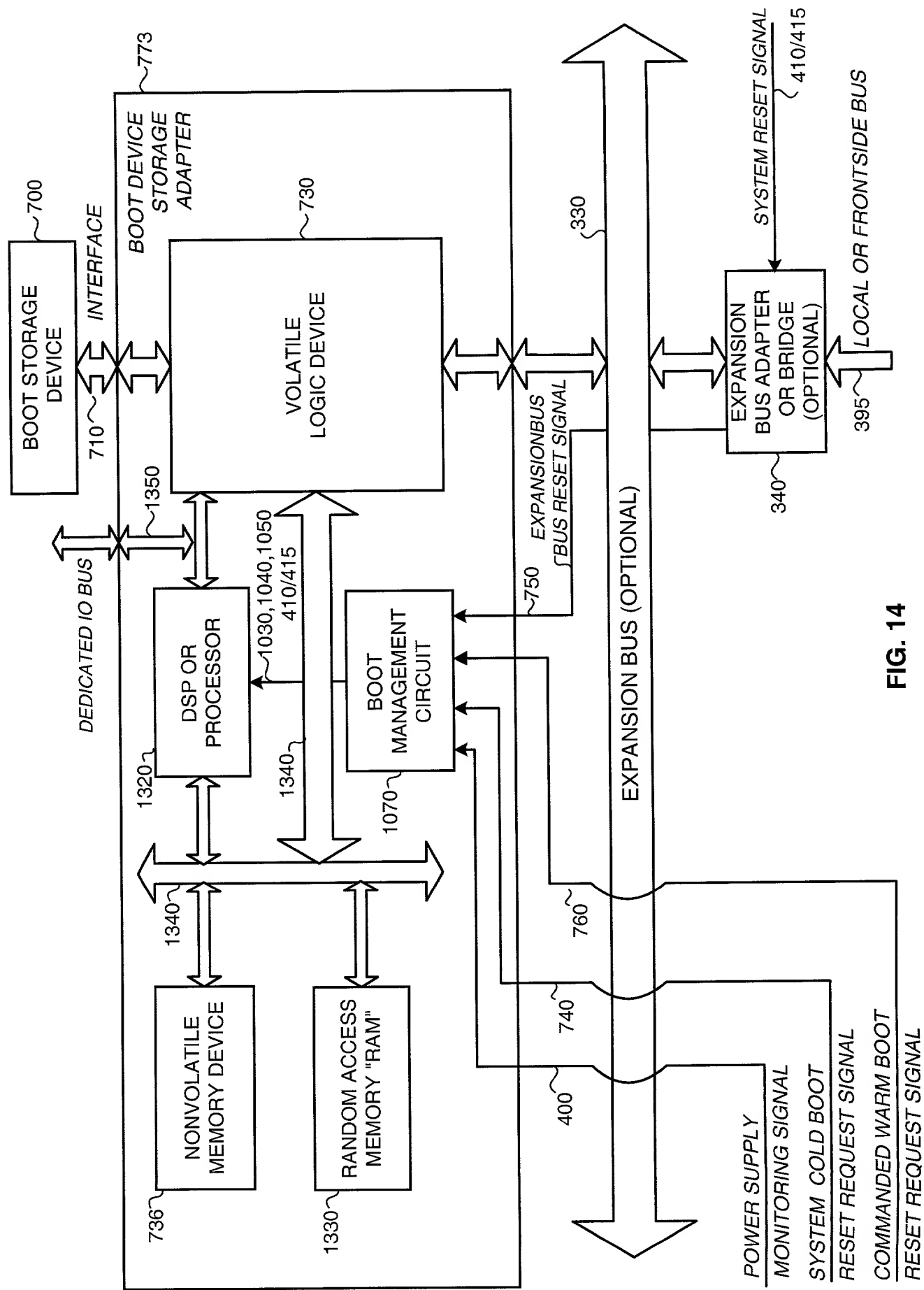


FIG. 14

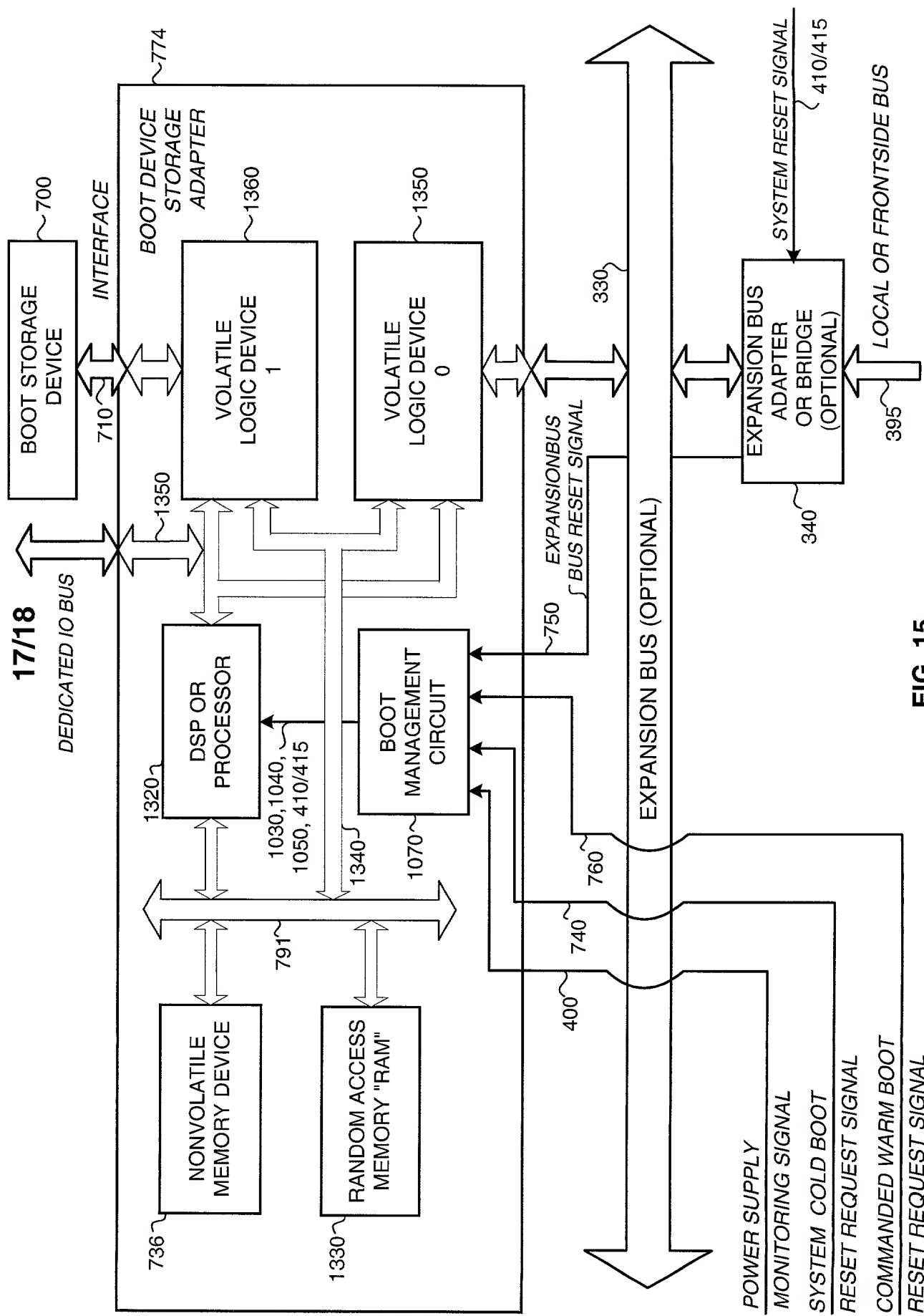


FIG. 15

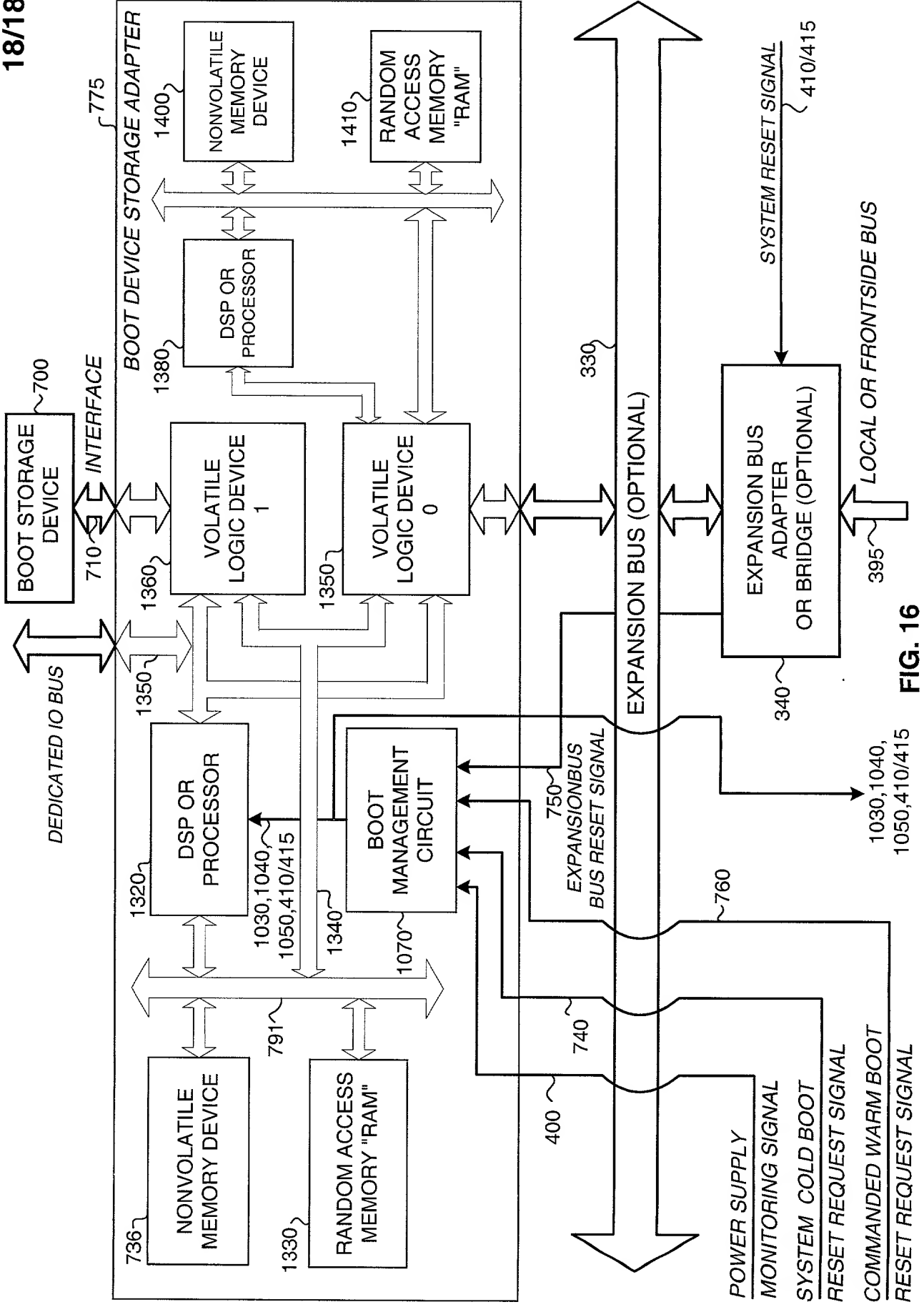


FIG. 16